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CLAIMS

1           1. A method of forming a semiconductor structure comprising:  
2           providing a single crystal semiconductor substrate of GaP; and  
3           fabricating a graded composition buffer including a plurality of epitaxial  
4           semiconductor  $\text{In}_x(\text{Al}_y\text{Ga}_{1-y})_{1-x}\text{P}$  alloy layers, said buffer comprising a first alloy layer  
5           immediately contacting the substrate having a lattice constant that is nearly identical to that  
6           of the substrate, subsequent alloy layers having lattice constants that differ from adjacent  
7           layers by less than 1%, and a final alloy layer having a lattice constant that is substantially  
8           different from the substrate, wherein growth temperature of the final alloy layer is at least  
9           20°C less than the growth temperature of the first alloy layer.

1           2. The method of claim 1, wherein growth temperature is decreased in at least one  
2           discrete transition during the growth of the graded composition buffer.

1           3. The method of claim 1, wherein the growth temperature of the first alloy is  
2           greater than or equal to 710°C.

1           4. The method of claim 2, wherein the growth temperature of the first alloy is  
2           greater than or equal to 710°C.

1           5. The method of claim 4, wherein first discrete transition in growth temperature  
2           ends in a growth temperature of 700° C or lower and occurs at a composition where x is  
3           between 0.05 and 0.35.

1           6. The method of claim 5, wherein a second discrete transition in growth  
2           temperature ends in a growth temperature of 650°C or lower and occurs at a composition  
3           where x is between 0.2 and 0.35.

1           7. The method of claim 6, wherein a third discrete transition in growth temperature  
2           ends in a growth temperature of 650°C or lower and occurs at a composition where x is  
3           between 0.3 and 0.6.

1           8. The method of claim 4, wherein a plurality of subsequent discrete transitions in  
2 growth temperature ends in a final growth temperature between 575 and 700°C.

1           9. The method of claim 4, wherein a plurality of subsequent discrete transitions in  
2 growth temperature ends in a final growth temperature between 480 and 560°C.

1           10. The method of claim 4, wherein a first discrete transition in growth temperature  
2 ends in a growth temperature of 560°C or lower and occurs at a composition where x is  
3 between 0.1 and 0.35.

1           11. The method of claim 2, wherein the growth temperature of the first alloy layer  
2 is greater than or equal to 750°C, a first discrete transition in growth temperature ends in a  
3 growth temperature of 675°C and occurs at a composition where  $x=0.18$ .

1           12. The method of claim 11 wherein a second discrete transition in growth  
2 temperature ends in a growth temperature of 650°C and occurs at a composition where  
3  $x=0.27$ .

1           13. The method of claim 12, wherein a third discrete transition in growth  
2 temperature ends in a growth temperature of 625°C and occurs at a composition where  
3  $x=0.4$ .

1           14. The method of claim 11, wherein a second discrete transition in growth  
2 temperature ends in a growth temperature between 525 and 550°C and occurs at a  
3 composition where x is between 0.25 and 0.35.

1           15. The method of claim 2, wherein the growth temperature of the first alloy layer  
2 is greater than or equal to 760°C, a first discrete transition in growth temperature ends in a  
3 growth temperature between 525 and 550°C and occurs at a composition where  $x=0.18$ .

1           16. The method of claim 1, wherein the substrate and the graded composition buffer  
2 are electrically doped with elements.

1 17. The method of claim 16, wherein the dopant elements comprise n-type dopants.

1 18. The method of claim 17, wherein the dopant element in the graded composition  
2 buffer comprises Si.

1 19. The method of claim 16, wherein the dopant elements comprise p-type dopants.

1 20. The method of claim 16, wherein the concentration of the dopant element in the  
2 alloy layers of the graded composition buffer is between  $5 \times 10^{16}$  and  $5 \times 10^{18} \text{ cm}^{-3}$ .

1 21. The method of claim 18 wherein the concentration of Si in the alloy layers of  
2 the graded composition buffer is between  $1 \times 10^{17}$  and  $5 \times 10^{18} \text{ cm}^{-3}$ .

1 22. The method of claim 2 wherein the substrate is electrically doped with an n-type  
2 dopant, the graded composition buffer is electrically doped with Si at a concentration  
3 between  $1 \times 10^{17}$  and  $2 \times 10^{18} \text{ cm}^{-3}$ , the growth temperature of the first alloy layer is greater  
4 than or equal to  $750^\circ\text{C}$ , a first discrete transition in growth temperature ends in a growth  
5 temperature of  $700^\circ\text{C}$  or lower and occurs at a composition where x is between 0.13 and 0.2.

1 23. The method of claim 1, wherein aluminum is present in the alloys ( $y > 0$ ) such  
2 that the grade composition buffer is transparent to light emitted or absorbed by  $\text{In}_x\text{Ga}_{1-x}\text{P}$   
3 lattice-matched to the final alloy layer.

1 24. The method of claim 23, wherein aluminum concentration in the alloy layers is  
2 such that y equals or is greater than 0.02.

1 25. The method of claim 23, wherein y equals or is greater than 0.05 beginning at  
2 a composition where x equals or is greater than 0.25.

1 26. The method of claim 23, wherein y equals or is greater than 0.05 beginning at  
2 a composition where x is at least 0.02 less than it is in the final alloy layer.

1           27. The method of claim 1, wherein semiconductor layers are incorporated on the  
2 graded composition buffer, and said layers comprise at least one strain-balancing  
3 semiconductor layer with nominally the same coefficient of thermal expansion as GaP.

1           28. The method of claim 27, wherein the strain balancing semiconductor layer  
2 comprises  $\text{In}_x(\text{Al}_y\text{Ga}_{1-y})_{1-x}\text{P}$  with a lattice constant smaller than that of the final alloy layer  
3 of the grade composition buffer.

1           29. The method of claim 28, wherein the strain balancing semiconductor layer is at  
2 least 5 microns in thickness.

1           30. The method of claim 27, wherein the strain balancing semiconductor layer  
2 comprises GaP.

1           31. The method of claim 30, wherein the strain balancing semiconductor layer  
2 comprises an epitaxial layer.

1           32. The method of claim 30, wherein the strain balancing semiconductor layer  
2 comprises a wafer-bonded layer.

1           33. The method of claim 30, wherein the strain-balancing semiconductor layer is at  
2 least 5 microns in thickness.

1           34. The method of claim 1, wherein additional layers are deposited on the graded  
2 composition buffer in order to fabricate optoelectronic devices thereon.

1           35. The method of claim 34, wherein at least one of the additional layers is an active  
2 layer whose purpose is to emit or absorb light.

1           36. The method of claim 35, wherein aluminum is present ( $y>0$ ) in the alloy layers  
2 of the graded composition buffer such that the graded composition buffer is transparent to  
3 light emitted or absorbed by the active layer or active layers.

1 37. The method of claim 36, wherein aluminum concentration in the alloy layers of  
2 the graded composition buffer is such that y equals or is greater than 0.02.

1 38. The method of claim 37, wherein y equals or is greater than 0.05 beginning at  
2 a composition where x equals or is greater than 0.25.

1 39. The method of claim 38, wherein y equals or is greater than 0.05 beginning at  
2 a composition where x is at least 0.02 less than it is in the final alloy layer of the graded  
3 composition buffer.

1 40. The method of claim 34, wherein the optoelectronic devices comprise light-  
2 emitting diodes.

1 41. The method of claim 34, wherein the optoelectronic devices comprise laser  
2 diodes.

1 42. The method of claim 34, wherein the optoelectronic devices comprise  
2 photodetectors.

1 43. The method of claim 34, wherein the optoelectronic devices comprise  
2 photocathodes.

1 44. The method of claim 34, wherein the optoelectronic devices comprise  
2 modulators.

1 45. The method of claim 1, wherein the alloy layers in the graded composition  
2 buffer comprise indium gallium phosphide where the lattice constant differs between  
3 adjacent layers by less than 0.2%, the substrate is electrically doped with an n-type dopant,  
4 the graded composition buffer is electrically doped with Si to a concentration of  $7 \times 10^{17} \text{ cm}^{-3}$ ,  
5 the first alloy layer of the graded composition buffer is grown at 800°C, the first discrete  
6 transition in growth temperature ends in a growth temperature of 675°C and occurs at a  
7 composition where  $x=0.18$ , the second discrete transition in growth temperature ends in a  
8 growth temperature of 650°C and occurs at a composition where  $x=0.26$ .

1           46. The method of claim 45, wherein a light-emitting diode is deposited after the  
2 final alloy layer of the graded composition buffer.

1           47. The method of claim 45, wherein a light-emitting diode is deposited after the  
2 final alloy layer of the graded composition buffer and a GaP strain-balancing layer is  
3 deposited with a thickness of at least 5 microns.

1           48. The method of claim 45, wherein a third discrete transition in growth  
2 temperature ends in a growth temperature of 625°C and occurs at a composition where  
3  $x=0.40$ .

1           49. The method of claim 48, wherein a light-emitting diode is deposited after the  
2 final alloy layer of the graded composition buffer.

1           50. The method of claim 48, wherein a light-emitting diode is deposited after the  
2 final alloy layer of the graded composition buffer and a GaP strain-balancing layer is  
3 deposited with a thickness of at least 5 microns.

1           51. The method of claim 1, wherein the alloy layers in the graded composition  
2 buffer comprise indium gallium phosphide where the lattice constant differs between  
3 adjacent layers by less than 0.2%, the substrate is electrically doped with an n-type dopant,  
4 the graded composition buffer is electrically doped with Si to a concentration of  $7 \times 10^{17} \text{ cm}^{-3}$ ,  
5 the first alloy layer of the graded composition buffer is grown at 800°C, the first discrete  
6 transition in growth temperature ends in a growth temperature of 675°C and occurs at a  
7 composition where  $x=0.18$ , and aluminum composition in the alloy layers is  $y=0.15$  for alloy  
8 compositions greater than or equal to  $x=0.25$ .

1           52. The method of claim 51, wherein additional layers are deposited on the final  
2 alloy layer of the graded composition buffer.

1           53. The method of claim 52, wherein the additional layers form the structure for a  
2 light-emitting diode.

- 1 54. The method of 53, wherein a strain-balancing GaP layer at least 5 microns in
- 2 thickness is deposited on the light-emitting diode structure.

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